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10/827,534	04/20/2004	Akira Ishikawa	740756-2724	5529

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EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,534	ISHIKAWA, AKIRA	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36,49-54 and 57-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36,49-54 and 57-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 11-14,16-19, 21-24, 26-29, 31-34, 36, 49-54, 57-60, 62-73, & 75 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang (US 5,814,529).

FIG. 5A

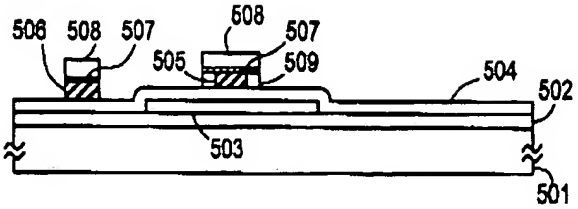


FIG. 5B

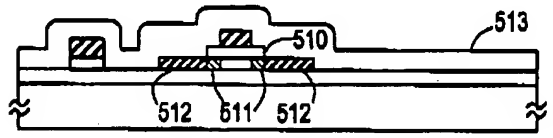


FIG. 5C

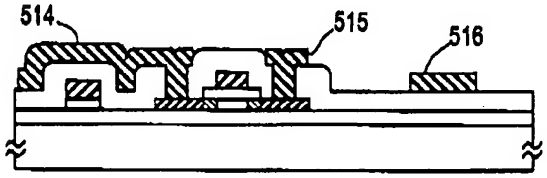


FIG. 5D

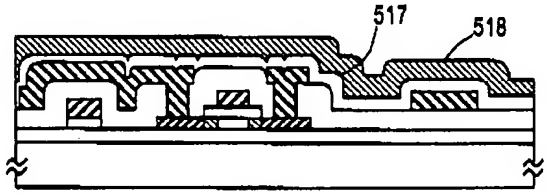


FIG. 5E

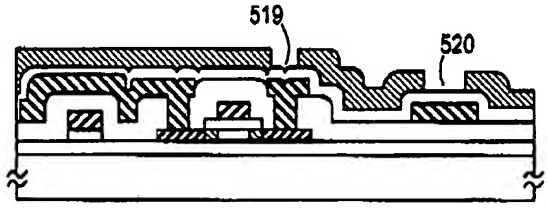
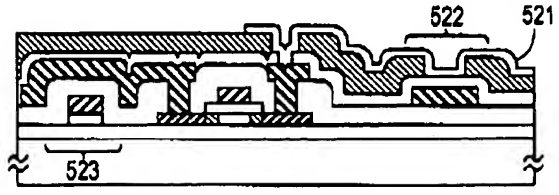


FIG. 5F



Regarding claims 1,2,3,4 & 49,50,51,52, Zhan teaches a method for manufacturing a semiconductor device comprising: forming a gate insulating film (Zhang, Fig 5A, [504]) over a semiconductor region;

forming a gate electrode (Zhang, Fig 5A, [505]) over the semiconductor region (Zhang, Fig 5A, [503]) with the gate insulating film interposed there between;

forming sidewalls covering at least sides of the gate electrode; (Zhang, Fig 5A, [509])

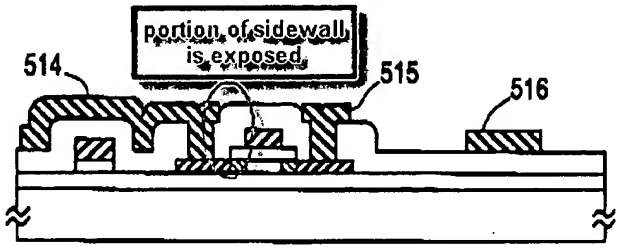
etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source and drain regions (Zhang, Fig 5B – [512]-source & drain - Figs. 5A→5B show that the sidewall 509 used as a mask to expose source and drain regions 512 prior to the formation of layer 513);

forming a conductive film over the semiconductor region after exposing the source and drain regions; ***The figure progression shows that potions of layer 513 is etched away to expose the "semiconductor region" 503 then a conductive film 514-516 is deposited making contact with the semiconductor region. This conductive film is being placed over the source and drain regions. (Col. 8 lines 18-22)***

removing an entire upper portion of the resist to expose an upper surface of the conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask; (Col. 6 lines 13-16, Zhang teaches that aluminum wiring layers are formed from a layer of Aluminum that is coated with a photoresist, the photoresist is formed into a mask, and then Aluminum film is etched into wiring layers. *Col. 8 lines 18-22 teach that the wiring pattern 514-516 is also formed from an Aluminum film by etching. It is inherently understood that this wiring layer is formed by the same method.)*

etching a portion of the conductive film by using the resist mask so that a portion of the sidewalls is exposed; and (Zhang, Fig 5C – see figure below)

FIG. 5C



etching a portion of the etched conductive film to form source and drain electrodes which are in contact with the source and drain regions (Zhang, Fig 5C –[514] & [515]).

Regarding claims 5,6 & 53,54, Zhan teaches a method for manufacturing a semiconductor device comprising: forming a first insulating film over a semiconductor region;

forming a first conductive film over the first insulating film;

forming a second insulating film over the first conductive film;

forming a hard mask by etching the second insulating film;

etching the first conductive film by using the hard mask as a mask to form a gate electrode; (Zhang, Col. 3, lines 8-34)

From Zhang, Fig. 1A, it is inherent that the gate electrode 106 had to be formed by a mask. The use of a hard mask as claimed, for forming a gate electrode is common practice in the art which is briefly described by Zhang, Col. 3, lines 8-34.

forming a third insulating film over the semiconductor region; (Zhang, Fig 5A, [513])

etching the third insulating film to form sidewalls covering at least sides of the gate electrode; (Zhang, Fig 5C)

etching the first insulating film by using the sidewall and the hard mask as a mask to form a gate insulating film and to expose an upper surface of the source and drain regions; (Zhang, Fig 1C-D, [110 & 113])

forming a second conductive film; (Zhang, *Col. 8 lines 18-22*)

forming a resist over the second conductive film; (Col. 6 lines 13-16 & *Col. 8 lines 18-22*)

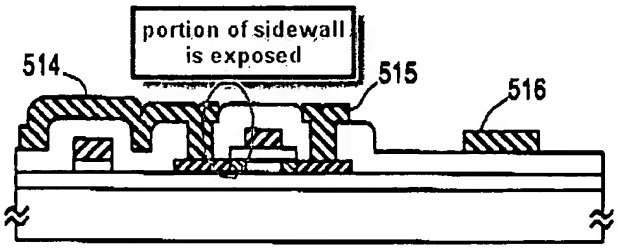
removing an entire upper portion of the resist to expose an upper surface of the conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask; (Col. 6 lines 13-16, Zhang teaches that aluminum wiring layers are formed from a layer of Aluminum that is coated with a photoresist, the photoresist is formed into a mask, and then Aluminum film is etched into wiring layers. *Col. 8 lines 18-22 teach that the wiring pattern 514-516 is also formed from an Aluminum film by etching. It is inherently understood that this wiring layer is formed by the same method.)*

etching a portion of the second conductive film by using the resist mask as a mask so that a portion of the sidewalls is exposed; and (Edwards, col. 4, lines 1-3)

etching a part of the etched second conductive film and a part of the semiconductor region to form a source and drain electrode (Zhang, Fig 1C-D, [116 & 117])

etching a portion of the second conductive film by using the resist mask as a mask so that a portion of the sidewalls is exposed (Zhang, Fig 5C – see figure below).

FIG. 5C



Regarding claim 7, Zhan teaches the method for manufacturing a semiconductor device according to Claim 1, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 8, Zhan teaches the method for manufacturing a semiconductor device according to Claim 1, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a portion of the conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 9, Zhan teaches the method for manufacturing a semiconductor device according to Claim 1, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A, [103]).

Regarding claim 11, Zhan in teaches the method for manufacturing a semiconductor device according to Claim 9, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A, [103]).

Regarding claim 12, Zhan teaches the method for manufacturing a semiconductor device according to Claim 2, wherein the resist mask is formed by developing after exposing an *entire face of the* resist to light (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 13, Zhan teaches the method for manufacturing a semiconductor device according to Claim 2, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 14, Zhan teaches the method for manufacturing a semiconductor device according to Claim 2, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A, [103]).

Regarding claim 16, Zhan teaches the method for manufacturing a semiconductor device according to Claim 14, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A, [103]).

Regarding claim 17, Zhan teaches the method for manufacturing a semiconductor device according to Claim 3, wherein the resist mask is formed by developing after exposing an entire face of the resist to light (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 18, Zhan teaches the method for *manufacturing* a semiconductor device according to Claim 3, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 19, Zhan the *method for manufacturing* a semiconductor device according to Claim 3, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A, [103]).

Regarding claim 21, Zhan teaches the method for manufacturing a semiconductor device according to Claim 19, *wherein* the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A, [103]).

Regarding claim 22, Zhan teaches the method for manufacturing a semiconductor device according to Claim 4, wherein the resist mask is formed by developing after exposing an entire face of the resist to light (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 23, Zhan teaches the method for manufacturing a semiconductor device according to Claim 4, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 24, Zhan teaches the method for manufacturing a semiconductor device according to Claim 4, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A, [103]).

Regarding claim 26, Zhan teaches the method for manufacturing *a* semiconductor device according to Claim 24, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A, [103]).

Regarding claim 27, Zhan teaches the method for manufacturing a semiconductor device according to Claim 5, wherein the resist mask is formed by developing after exposing an entire face of the resist to light (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 28, Zhan teaches the method for manufacturing a semiconductor device according to Claim 5, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the second conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 29, Zhan teaches the method for manufacturing a semiconductor device according to Claim 5, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A, [103]).

Regarding claim 31, Zhan teaches the method for manufacturing a semiconductor device according to Claim 29, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A, [103]).

Regarding claim 32, Zhan teaches the method for manufacturing a semiconductor device according to Claim 6, wherein the resist mask is formed by developing after exposing an entire face of the resist to light ((Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 33, Zhan teaches the method for manufacturing a semiconductor device according to Claim 6, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the second conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 34, Zhan teaches the method for manufacturing a semiconductor device according to Claim 6, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A, [103]).

Regarding claim 36, Zhan teaches the method *for* manufacturing *a* semiconductor device according to Claim 34, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A, [103]).

FIG. 1A

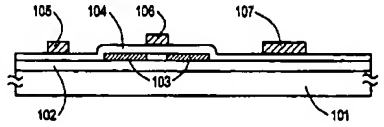


FIG. 1B

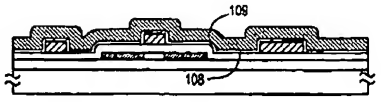


FIG. 1C

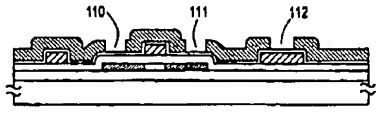


FIG. 1D

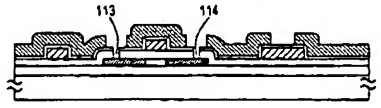
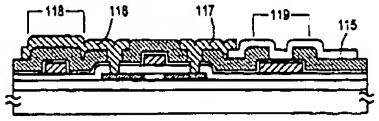


FIG. 1E



Regarding claims 57,64 & 63,69, Zhan teaches a method for manufacturing a semiconductor device comprising:

forming a gate insulating film over a semiconductor region; (Zhang, Fig 1A)

forming a gate electrode over the semiconductor region with the gate insulating film interposed there between; (Zhang, Fig 1A)

forming an insulating film covering the gate electrode;

etching a portion of the insulating film to expose a portion of the semiconductor region and to form portions of the insulating film remaining on at least side surfaces of the gate electrode; (Zhang, Fig 1A-E, [110 & 113])

etching the gate insulating film by using the remaining portion of the insulating film as a mask to expose an upper surface of the source and drain regions:

forming a conductive film over the semiconductor region after exposing the source and drain regions; (Zhang, Fig 1A-E, [116])

forming a resist over the conductive film;

removing an entire upper portion of the resist to expose an upper surface of the conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask; (Col. 6 lines 13-16, Zhang teaches that aluminum wiring layers are formed from a layer of Aluminum that is coated with a photoresist, the photoresist is formed into a mask, and then Aluminum film is etched into wiring layers. *Col. 8 lines 18-22 teach that the wiring pattern 514-516 is also formed from an Aluminum film by etching. It is inherently understood that this wiring layer is formed by the same method.)*

etching a portion of the conductive film by using the resist mask so that a portion of the insulating film is exposed; and (Zhang, Fig 5C)

etching a portion of the conductive film by using the resist mask so that a portion of the remaining portion of the insulating film is exposed; and

etching a part of the etched conductive film to form source and drain electrodes which are in contact with the source and drain regions, and (Edwards, col. 3-4, lines 74-3)

wherein said the source and drain regions are outside of the remaining portion of the insulating film (Zhang, Fig 1A-E, [103])

wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of the source and drain regions (Zhang, Fig 1A-E, [103]).

Regarding claim 58, Zhan a method for manufacturing a semiconductor device according to Claim 57, wherein the resist mask is formed by developing after exposing an entire face of the resist to light (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 59, Zhan in view of Edwards teaches a method for manufacturing a semiconductor device according to Claim 57, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film (Edwards, col. 3-4, lines 74-3).

Regarding claim 60, Zhan teaches a method for manufacturing a semiconductor device according to Claim 57, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A-E, [103]).

Regarding claim 62, Zhan teaches a method for manufacturing a semiconductor device according to Claim 60, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A-E, [103]).

Regarding claim 65, Zhan teaches a method for manufacturing a semiconductor device according to Claim 64, wherein the resist mask is formed by developing after exposing an entire face of the resist to light (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 66, Zhan teaches a method for manufacturing a semiconductor device according to Claim 64, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 67, Zhan teaches a method for manufacturing a semiconductor device according to Claim 64, wherein the semiconductor region is a semiconductor thin film (Zhang, Fig 1A-E, [103])

Regarding claim 68, Zhan teaches a method for manufacturing a semiconductor device according to Claim 67, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A-E, [103]).

Regarding claims 70 & 76, Zhan teaches a method for manufacturing a semiconductor device comprising: forming a gate insulating film over a semiconductor region including source and drain regions; (Zhang, Fig 1A, [104])

forming a gate electrode over the semiconductor region with the gate insulating film interposed there between; (Zhang, Fig 1A)

forming sidewalls covering at least sides of the gate electrode; (Zhang, Fig 1B, [109])

etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source an drain regions;

forming a first conductive film over the semiconductor region after exposing the sorce and drain regions; (Zhang, Fig 1A-E, [116])

forming a resist over the first conductive film;

removing an entire upper portion of the resist to expose an upper surface of the first conductive film, said upper surface being located over the gate electrode, therby leaving a resist mask;

etching a portion of the first conductive film by using the resist mask to form a second conductive film; (Edwards, col. 3-4, lines 74-3)

etching a part of the second conductive film to form a source electrode and a drain electrode, (Zhang, Fig 1E, [116 & 118])

forming an interlayer insulating film over the source electrode and the drain electrode, and (Zhang, Fig 3C, [311])

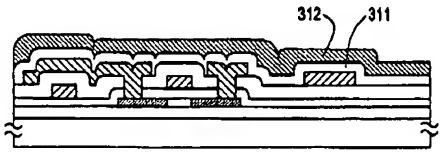
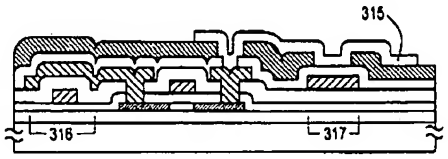
FIG. 3C 

FIG. 3E 

forming at least one connection wiring over the interlayer insulating film, (Zhang, Fig 3E, [315])

wherein said connection wiring is connected to one of the source electrode and the drain electrode through a hole of the interlayer insulating film.

wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of the source and drain regions. (Zhang, Fig 1E shows the electrodes 118 & 116 in contact with a upper and side source and drain regions).

Regarding claim 71, Zhan teaches a method for manufacturing a semiconductor device according to Claim 70, wherein the resist mask is formed by developing after exposing an entire face of the resist to light (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 72, Zhan teaches a method for manufacturing a semiconductor device according to Claim 70, wherein the resist mask is formed by etching an entire

face of the resist, and exposing a part of the conductive film (Col. 6 lines 13-16 & *Col. 8 lines 18-22*).

Regarding claim 73, Zhan teaches a method for manufacturing a semiconductor device according to Claim 70, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film (Zhang, Fig 1A-E, [103]).

Regarding claim 75, Zhan teaches a method for manufacturing a semiconductor device according to Claim 73, wherein the semiconductor thin film is a crystalline silicon film (Zhang, Fig 1A-E, [103]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 15, 20, 25, 30, 35, 61, & 74are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 5,814,529), in view of Edwards (US 3,189,973).

Regarding claims 10, 15, 20, 25, 30, 35, 61, & 74, Zhan teaches the method for manufacturing a semiconductor device according to Claims 9, 14, 19, 24, 29, 34, 60, & 73, however does not explicitly disclose wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. Using single crystal Si substrates is conventional for forming TFTs. For example Edwards (Col. 4, line 3) uses a single crystal silicon substrate.

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Zhan and Edwards to enable the providing a substrate step of Zhan to be performed according to the teachings of Edwards because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of performing the disclosed providing a substrate step of Zhan and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Zhan discloses the claimed invention except for the use of a Si substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a Si substrate, since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JJS
August 2, 2006

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